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SiO_x Layers for Nanoscale Device Application Grown on RF Plasma Hydrogenated (100) and (111) Silicon

S. Alexandrova[1], **A. Szekeres**[2], **E. Halova**[1], **N. Kojuharova**[1]

[1]Department of Applied Physics, Technical University of Sofia, 1797 Sofia, Bulgaria
[2]Institute of Solid State Physics, Bulgarian Academy of Sciences, 1784 Sofia, Bulgaria

Abstract. The most important issue in modern semiconductor devices is the characterization and limiting of the defects at the interfaces in single or multilayered structures. The process of hydrogenation in Si technology has been used due to beneficial effects such as stabilization of device characteristics through gettering of impurities and saturation of defects. In future nanoelectronic applications, exfoliation of silicon in smart cut process, increase carrier life time in solar cells, etc. it is expected to find even growing interest.

The aim of the present paper is characterization of the interface defects between rf plasma hydrogenated (100) p-Si and (111) n-Si wafers and the overgrown SiO_x ($x < 2$). The plasma hydrogenation of the Si wafers was conducted at different substrate temperatures. The Si/SiO_x structures were built in MOS capacitors. The interface defects were examined in detail.

The information on interface traps density was gained by two C-V based techniques. The first classical one uses comparison of theoretically calculated and measured C-V characteristics. The second one is based on analysis of C-V and G-V characteristics, taken at frequencies ranging from 10 to 200 kHz, in order to obtain a generalized C-V curve. In this curve the series resistance and the leakage through the oxide layer is accounted for. Ellipsometric data and capacitance in strong accumulation of the C-V curves were used for calculation of the thickness and the dielectric constants of the oxide layers. The SiO_x thickness varied depending on the hydrogenation level and Si orientation but remained in the nanoscale range in the order below 10 nm. The oxide density of the SiO_x layers and the stoichiometry factor x have been estimated.

The analysis of the C-V and G-V curves has shown that SiO_x layer grown on Si treated in plasma exhibit small oxide charge and low leakage currents required for high quality dielectric layers. Comparative analysis from the application of the two C-V techniques used to extract the interface spectra has been conducted. The results have shown the presence of localized traps energetically distributed in the Si bandgap. The positions and the density of the trap levels in the Si bandgap depend

on substrate orientation and on hydrogenation temperature. The density around midgap from both techniques show low levels as needed for nanoscaled devices. The traps near band edges reveal a set of states (border traps) with positions and density that depend on the different preparation conditions. Variations are also observed depending on data yielded by the two C-V techniques due to contribution of the trap response time to data analysis.

Interpretation of the interface trap density spectra relates the localized interface traps on the amount of incorporated hydrogen and is related to particular structural defects in a thin interface region inside the oxide.